**Steen Larsen**

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**CPU Architect | Platform Architect**

Innovative CPU Architect with extensive experience defining and optimizing advanced server, platform, and IP architectures for Intel Datacenter, with expertise spanning micro-architecture design, SoC-level features, and high-impact problem-solving. Demonstrated success in developing architecture specifications, leading cross-functional collaboration, and resolving critical issues for platforms. Adept at balancing complex technical priorities and customer requirements to deliver market-driven, cost-effective solutions that enhance performance, scalability, and reliability.

**Core Competencies**

CPU Architecture | SoC Design | Micro-Architecture | Performance Optimization

Memory Coherency | SystemVerilog RTL | Agile Methodology | Presilicon Postsilicon Debugging and Testing

Platform Architecture | Latency and Power analysis| Kernel Cloud Dev | AI workloads | Stakeholder Collaboration

**Experience**

**Intel Corporation**

**Server and IP Architect July 2022 - October 2024**

Defined architecture in a Hardware Architecture Specification (HAS) and resolved customer architecture issues and questions. Detailed at a level micro-architecture and SystemVerilog RTL design engineers can implement as well as chip (SoC) level architecture can utilize new features for higher level performance, power, cost and features including RAS, debug, test, security, boot/config/power flows, etc.

* UCIe (Universal Chiplet Interconnect Express) Die-to-Die IP block owner, documenting HAS, register functionality and definition for usage by FW and validation trading off priorities on security, RAS, power, performance, features to meet timeline requirements for a 2027 CPU product.
* ULA (UPI Link Agent IP) co-owner driving issue resolution and focusing on link encryption, security, RAS and performance counter definition.
* IOMMU (IO Memory Management Unit) co-owner writing coherent memory write cache specification, drafting debug, negative space validation architecture content and VTd specification feature alignment.
* Solved hard relevant problems of impact, documenting clearly and unambiguously how to implement RTL logic, FSMs and validation, with smart people for market-driven consumers.

**OS cloud solutions kernel performance and Lead Engineer November 2021 - June 2022**

Virtual machine memory performance optimization and tuning involving NUMA and sub-NUMA cluster, load migration controls, analysis and comparisons to end customer usage.

* Coded kernel debug and monitoring hooks between near-memory DRAM pages, far-memory persistent memory pages, and SSD swapping to characterize performance optimizations.
* Defined characterization and judgment of critical factors in analysis and conclusion/recommendations (HammerDB, SPECjbb, etc.) using flamegraphs and resource utilization and scaling analysis.
* Tuned current generation and influenced future generation architecture and cloud orchestration, etc.

**Entry Server Lead Platform Architect, Lead System Engineer, Platform Execution Board Lead 2016 - 2021**

Defined Catlow’23 and delivered Mehlow’18 and Tatlow’21 platform architecture definition and grading specifying how entry server technology components meet marketing and customer requirements. Authored the architecture specifications, represented architecture in planning and execution sessions, and incorporating planning/marketing/customer feedback to develop highly profitable products.

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* Platform Status Reviews (PSR) and direct face-to-face customer interactions (Apple/HPE/HPI/Dell/Lenovo) to represent rapid in-room technical expertise with customer requests within given constraints.
* Proposed and drove adoption of a refined entry server power management (PM-lite) to reduce PL2 ratio to PL1 from client-biased >1.8X to datacenter target of 1.2X quantifying performance impact based on customer feedback and technology constraints. This addresses invalid thermal event reporting to server management over PECI and avoiding a silicon change saving millions in development costs.
* Led regular meeting discussions with client platform and silicon arch (CPU and PCH) to position datacenter architecture requests in appropriate context. (i.e. drove PCH-H RTL change to support NMI/SMI forwarding). This enabled alignment of feature scheduling and resource optimization.
* Provided platform arch support for Jackson Falls and Fishhawk Falls workstation platforms. This involved ensuring workstation interests were properly reflected in server CPU architecture definitions.

**Shared Memory Research Engineer and Pathfinding August 2015 - April 2016**

ScaleMP-based proof-of-concept of shared memory and performance impact of non-local memory and prefetcher capabilities to cover latencies.

* Shared memory HW architecture specification with Markov models (M/D/1 and M/M/n) to define performance projections based on fabric capacities and latency sensitivities.
* Benchmarked latency impacts with node-to-node latencies over efficient prefetch implementations on Hadoop/SPARK, SAP-H, CPU2017, and ML algorithms.
* Cross-compared Omnipath with ROCE 100GbE RDMA measurements and root caused the added ~120ns end-to-end latency increase as MPI SW overheads (based on consensus of architecture experts)

**Additional Relevant Experience**

**Various Intel division roles:**

**board signal integrity engineer, emulation validation engineer (Veloce | SystemVerilog), network research scientist, board design engineer, pre-silicon validation engineer, FPGA/ASIC design**

**Education**

**Doctor of Philosophy (PhD), Electrical and Computer Engineering**

Oregon State University

* Dissertation on platform PCIe I/O latency reduction, root port bypass, and power optimization. 10GbE and PCIe AMBA AXI IP with optimized assembly driver coding for write-combining buffer utilization and UDP/IP offload engine.

**Management in Science and Technology, (MST)**

OHSU/OGI

**Master of Science (MS), Electrical and Computer Engineering**

Oregon State University

**Bachelor of Science (BS), Computer Engineering**

Oregon State University

**Publications and References**

* 6 papers and 28 patents granted <https://scholar.google.com/citations?user=UWLeXOAAAAAJ>
* Please see https://www.linkedin.com/in/steenknudlarsen/